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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/000,626	12/30/97	RENGARAJAN, R	97/P/7971/US

MM21/0224

SIEMENS
INTELLECTUAL PROPERTY DEPARTMENT
186 WOOD AVENUE SOUTH
ISELIN NJ 08830

EXAMINER	
TRAN, T	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 02/24/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

1- File Copy

Office Action Summary	Application No. 09/000,626	Applicant(s) Rengarajan et al.
	Examiner Thien Tran	Group Art Unit 2811

☐ Responsive to communication(s) filed on _____.

☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-23* is/are pending in the application.

Of the above, claim(s) *12-23* is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-11* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Objections

1. Claim 9 is objected to because of the following informalities: line 3, "respresentative" should be --representative--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuda in view of Wolf.

Regarding claims 1, 8, 9 and 11, Fukuda discloses a trench isolation structure in Figs. 4(a)-4(e) comprising a V-shaped trench in a substrate 10, a silicon nitride liner 12' formed on the bottom of the trench, and a polysilicon 5 filled in the trench. Fukuda uses a polysilicon layer to fill the trench. However, both polysilicon layer and dielectric layer (TEOS) have been used for trench refill in the art. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute an equivalent dielectric layer (TEOS) for polysilicon since the examiner takes Official Notice of the equivalence of dielectric layer (TEOS)

and polysilicon for their use in the art and the selection of any of these known equivalents to fill the trench would be within the level of ordinary skill in the art.

Fukuda does not explicitly disclose a transistor disposed in a well beside the shallow trench isolation structure. However, it is old and well known in the art that shallow trench isolation structures are formed in the substrate to define an active region that includes a transistor and source/drain regions that define a channel region. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form a transistor in an active region beside the trench isolation structure.

Fukuda does not explicitly disclose the uppermost surface of the nitride liner is disposed below a transistor channel depth. Wolf discloses a shallow trench isolation structure formed in the substrate (5000-8000 angstroms deep) (page 45, line 28) is much deeper than source and drain junction depths (smaller than 2500 angstroms) (page 154, line 6). Trench isolation structures are routinely formed much deeper than the source/drain regions or channel region for obvious reasons. A nitride liner is formed on the bottom of the trench as taught by Fukuda. Therefore, it is obvious Fukuda's device provides a nitride liner below the transistor channel depth.

Regarding claims 2, 6 and 7, Fukuda does not specifically disclose a P-FET transistor. It is old and well known in the art to form trench isolation structure in the support circuitry with P-FET transistors generally employed.

Regarding claim 3, Fukuda does not explicitly disclose a nitride liner wherein the uppermost surface is disposed greater than 1000 angstroms below a top surface of the substrate. It would be an obvious matter of design choice to select the depth of the uppermost surface of the nitride liner since it is depended on the trench's depth. The trench's depth may vary with specific designs. Trench's depth in semiconductor devices is an art recognized variable of importance which is subject to routine experimentation and optimization. Accordingly, it would be well for one within ordinary skill in the art to select the depth of the uppermost surface of the nitride liner as taught by Fukuda in association with the trench's depth selection.

Regarding claims 4 and 5, Fukuda discloses a silicon dioxide film 11' formed on the surface of the trench and under the nitride liner 12'. Fukuda's device as described above has a dielectric layer (TEOS) extending to a top surface of the substrate and completely fills the trench.

Regarding claim 10, Fukuda does not specifically disclose a P-FET transistor. It is old and well known in the art to form trench isolation structure in the support circuitry with P-FET transistors generally employed. Fukuda does not explicitly disclose a channel depth is about 1000 angstroms below a top surface of the substrate. It would be an obvious matter of design choice to select the channel depth. Channel depth in semiconductor devices is an art recognized variable of importance which is subject to routine experimentation and optimization. Accordingly, it would be well for one within ordinary skill in the art to select the channel depth as taught by Fukuda. The claim limitation "said nitride liner may trap substantially no charge traversing said channel of said P-FET transistor" is a functional language and is given no patentable weight since it has

been held that claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).

Response to Arguments

4. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien Tran whose telephone number is (703) 308-4108.

Tom Thomas
Supervisory Patent Examiner
Technology Center 2800

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February 10, 1999